REMARKS

The Office Action dated November 14, 2007 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1, 2, 7, 11-13, 17, 19-26 and 28-36 have been amended to more particularly point out and distinctly claim the subject matter which is the invention. No new matter has been added. Claims 1-5, 7-15, 17-26 and 28-36 are submitted for consideration.

Claims 7 and 17 were objected to because of informalities. Claims 7 and 17 have been amended to overcome the objection. Therefore, Applicant requests that the objection be withdrawn.

Claims 1-5, 7-15, 17-20, 26, 28-32, 33, 34 and 36 were rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. Applicant submits that each of the pending claims previously recited each essential step, as required for the present invention. Nevertheless, claims 1-5, 7-15, 17-20, 26, 28-32, 33, 34 and 36 have been amended to overcome the rejection. Therefore, Applicant requests that the rejection be withdrawn.

Claims 21-24, 32 and 35 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,790,608 to Benayoun (hereinafter Benayoun). Claim 25 was rejected under 35 U.S.C. 103(a) as being unpatentable over Benayoun. In making the obviousness rejection, the Office Action took the position that Benayoun teaches all

of the elements of claim 25 except for teaching "the frequencies of the internal or external clocks." However, the Office Action alleged that "the frequencies of the internal or external clocks" would have been obvious to one skilled in the art. The rejections are traversed as being based on a reference that does not teach or suggest each of the elements of claims 21-25, 32 and 35.

Claim 21, upon which claims 22-25 depend, recites an apparatus including a plurality of dividers wherein an external synchronization input is applied to one of the plurality of dividers which is configured to generate an external timebase. The apparatus also includes an internal clock generator configured to generate a symbol clock. The symbol clock from the internal clock generator is applied to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase. The apparatus further includes a phase difference generator configured to generate phase difference information indicating a phase difference between the internal timebase and the external timebase. The internal timebase and the external timebase are applied to start and stop input of the phase difference generator. The apparatus also includes a symbol generator to which the phase difference is applied. The symbol generator is also configured to receive the symbol clock generated by the internal clock generator. The symbol generator is also configured to generate at least one of packets or symbols which include information on the phase difference. The apparatus further includes a transmitter configured to transmit the packets or symbols, which

include the information on the phase difference, generated by the symbol generator, to a receiver.

Claim 32 recites a method including applying an external synchronization input to one of a plurality of dividers which is configured to generate an external timebase and applying a symbol clock from an internal clock generator to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase. The method also includes generating, by a phase difference generator phase difference information indicating a phase difference between an internal clock and an external clock. The internal timebase and the external timebase are applied to start and stop input of the phase difference generator. The method also includes applying the phase difference to a symbol generator. The symbol generator is also configured to receive a symbol clock generated by an internal clock generator. The symbol generator is also configured to generate at least one of packets or symbols which include information on the phase difference. The method further includes transmitting, by a transmitter, the packets or symbols, which include the information on the phase difference, generated by the symbol generator, to a receiver.

Claim 35 recites an apparatus including applying means for applying an external synchronization input to one of a plurality of dividers which is configured to generate an external timebase and applying a symbol clock from an internal clock to another one of the plurality of dividers which is configured to generate an internal timebase of the same frequency as the external timebase. The apparatus also includes a phase difference

generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock. The internal timebase and the external timebase are applied to start and stop input of the phase difference generating means. The apparatus further includes applying means for applying the phase difference to a symbol generator. The symbol generator is also configured to receive a symbol clock generated by an internal clock generator. The symbol generator is also configured to generate at least one of packets or symbols which include information on the phase difference. The apparatus also includes a transmitting means for transmitting the packets or symbols, which include the information on the phase difference, generated by the symbol generator, to a receiver.

As outlined below, Benayoun does not teach or suggest each of the elements of claims 21-25, 32 and 35.

Benayoun discloses a method for synchronizing the clock signal of a first data terminal equipment to a second data terminal equipment connected to a communication network through a first network node and a second network node. The communication network has a reference clock (clock 1) that it transmits to the second network node which compares it with the clock signal (clock 2) it receives from the second data terminal equipment.

In Figure 6 of Benayoun, in case the rising edge or the up transition of clock 1 is earlier than the one of clock 2, the frequency of clock 1 is divided by 80 in a first divider circuit. Afterwards, the resulting clock signal is then received by the first 7-bit-counter,

the eighth bit being dedicated to the sign. The first counter stops on the rising edge of a clock signal issued by a divider, the clock signal being the clock signal CLK2 divided by 10. This first counter is clocked by an oscillator which generates a clock signal whose frequency is for example 10 times greater than clock 1. The output of the first counter is a 7-bit length word Q0-Q6 transmitted on a parallel bus representing the value digitally coded of the phase difference between clocks 1 and 2 to a first buffer. In the same way, in case the rising edge of clock 2 is earlier than the one of clock 1, a second 7-bit counter is enabled.

Applicant submits that Benayoun does not teach or suggest each of the elements of claims 21-25, 32 and 35. Each of claims 21-25, 32 and 35, in part, recites includes applying the phase difference to a symbol generator, the symbol generator being configured to receive a symbol clock generated by an internal clock generator. Each of claims 21-25, 32 and 35 also recites that the symbol generator is also configured to generate at least one of packets or symbols which include information on the phase difference. Benayoun does not teach or suggest these features.

In Benayoun, in particular Figure 6, the clock impulses CLK 1, CLK 2 of the dividers 300 and 310 are <u>not</u> applied to any symbol generator which receives a phase difference. In Figure 6 of Benayoun, the 7-bit counters 340 and 350 output the counting values to components 370 and 380. However, these components 370 and 380 do not receive any of the clocks CLK 1 or CLK 2. Contrary to Benayoun, each of claims 21-25, 32 and 35 recites a symbol generator which not only receives and packetizes the phase

difference information, but additionally receives the symbol clock generated by the internal clock generator.

Fig. 6 of the present application shows an embodiment of the invention where in block 60 TX, the symbol clock generated by the internal free running clock 60 is applied not only to the divider 65, but also to the packet/symbol generator 66, which packet/symbol generator 66 also receives the difference output generated by difference counter 63. The present application also discloses that the packet and/or symbol generator 66 generates packets and/or symbols which include the information on the phase difference between the internal and external time base and thus, between the internal and external clocks. As noted above, Benayoun does not teach or suggest these features.

Based on the distinctions noted above, Applicant requests that the rejections under 35 U.S.C. 102(b) and 103(a) be withdrawn because Benayoun does not teach or suggest each of the elements of independent claims 21, 32 and 35. Claims 22-25 depend on claim 21 and should be allowable at least for their dependence on claim 21, in addition to the further limitations recited in claims 22-25.

Claim 28 was rejected under 35 U.S.C. 103(a) as being unpatentable over Benayoun in view of U.S. Patent No. 7,106,224 to Knapp (hereinafter Knapp). According to the Office Action, Benayoun discloses all of the elements of claim 28 except for disclosing "multiplying, by the receiver, the frequency of the adjusted frequency-divided clock for generating an external clock." Therefore, the Office Action combined the teachings of Benayoun and Knapp in an effort to yield all of the elements

of claim 28. The rejection is traversed as being based on references that do not teach or suggest each of the elements of claim 28.

Claim 26, upon which claim 28 depends, was not rejected over Benayoun and Knapp. Therefore, the rejection of claim 28 is improper in view of the fact that claim 28 includes all of the limitations recited in claim 26.

Furthermore, Applicant notes that in the Office Action dated July 12, 2007, claims 9 and 10 were indicated to be allowable. Claims 9 and 10 previously recited storing, by the receiver, at least two successive values of the phase difference information received from the transmitter and detecting, by the receiver, a difference between the successive values of phase difference information. These allowable features are now recited in claim 26. There is no disclosure in Benayoun of storing, by the receiver, at least two successive values of the phase difference information received from the transmitter and detecting, by the receiver, a difference between the successive values of phase difference information.

Knapp does not cure the deficiencies of Benayoun, as outlined above. Specifically, Knapp does not teach or suggest recites storing, by the receiver, at least two successive values of the phase difference information received from the transmitter and detecting a difference between the successive values of phase difference information, as recited in claim 26, upon which claim 28 depends. Therefore, Applicant requests that the rejection under 35 U.S.C. 103(a) be withdrawn because neither Benayoun nor Knapp, whether taken singly or combined, teaches or suggests each of the elements of claim 26.

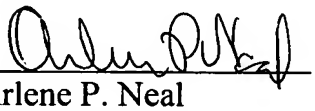
Claim 28 depends on claim 26 and should be allowed at least for its dependence on claim 26 in addition to the further limitations recited in claim 28.

According, Applicant submits that claims 1-5, 7-15, 17-26 and 28-36 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 1-5, 7-15, 17-26 and 28-36 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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